What is claimed is:

1. A temperature detecting circuit comprising:
a first, second and third voltage divider, each of which comprises resistors having temperature-dependent resistances, outputting a first, second and third voltage; and
a voltage comparator comparing the first voltage with the second voltage, and the first voltage with the third voltage and respectively outputting a first and second signal according to the comparison results.

2. The circuit as in claim 1, wherein the voltage comparator comprises:
a first transistor of a first type having a source coupled to receive a first voltage;
a second transistor of the first type having a gate coupled to a gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a first bit of a temperature detection signal;
a third transistor of the first type having a gate coupled to the gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a second bit of the temperature detection signal;
a fourth transistor of a second type having a drain coupled to a drain of the first transistor;

a fifth transistor of the second type having a drain coupled to the drain of the second transistor and a source coupled to a source of the fourth transistor;

a sixth transistor of the second type having a drain coupled to the drain of the third transistor and a source coupled to the source of the fourth transistor; and

a seventh transistor of the second type having a drain coupled to the drain of the fourth transistor, a gate coupled to receive an enable signal and a source coupled to receive a second voltage.

3. The circuit as in claim 2, wherein the voltage divider comprises:

a first resistor coupled between the gate of the fourth transistor and the source of the first transistor;

a second resistor coupled between the gate of the fourth transistor and the source of the seventh transistor;

a third resistor coupled between the gate of the fifth transistor and the source of the first transistor;

a fourth resistor coupled between the gate of the fifth transistor and the source of the seventh transistor;

a fifth resistor coupled between the gate of the sixth transistor and the source of the first transistor; and

a sixth resistor coupled between the gate of the sixth transistor and the source of the seventh transistor.

4. The circuit as in claim 2, wherein the first and second types are P and N type, respectively.

5. The circuit as in claim 2, wherein the first and second voltages are Vdd and a ground voltage, respectively.

6. The circuit as in claim 3, wherein the first, fourth, fifth and sixth resistors are made of poly-silicon.

7. The circuit as in claim 3, wherein the second and third resistors are parasitic resistances of an N well.

8. A circuit for controlling a self-refresh period of a semiconductor memory device, comprising:

a pulse generating circuit which outputs a periodic pulse train in response to an external control signal;

a frequency-dividing circuit which outputs a plurality of pulse trains having different periods from each other by frequency-dividing said periodic pulse train output by said pulse generating circuit;

a temperature detecting circuit which detects an ambient temperature of said memory device and outputs a temperature detection signal when said ambient temperature reaches a predetermined temperature level, the temperature detection circuit comprising:

a first transistor of a first type having a source coupled to receive a first voltage;

a second transistor of the first type having a gate coupled to a gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a first bit of the temperature detection signal;

a third transistor of the first type having a gate coupled to the gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a second bit of the temperature detection signal;

a fourth transistor of a second type having a drain coupled to a drain of the first transistor;

a fifth transistor of the second type having a drain coupled to the drain of the second transistor and a source coupled to a source of the fourth transistor;

a sixth transistor of the second type having a drain coupled to the drain of the third transistor and a source coupled to the source of the fourth transistor;

a seventh transistor of the second type having a drain coupled to the drain of the fourth transistor, a gate coupled to receive an enable signal and a source coupled to receive a second voltage; and

six resistors respectively coupled between the gate of the fourth transistor and the source

of the first transistor, the gate of the fourth transistor and the source of the seventh transistor, the gate of the fifth transistor and the source of the first transistor, the gate of the fifth transistor and the source of the seventh transistor, the gate of the sixth transistor and the source of the first transistor, the gate of the sixth transistor and the source of the seventh transistor;

a voltage detection circuit which detects a power supply voltage applied to said memory device and outputs a voltage detection signal when said power supply voltage reaches a predetermined voltage level; and,

a pulse selection circuit which outputs a self-refresh master clock by selecting one of said pulse trains in response to said temperature detection signal and said voltage detection signal.

9. The circuit as in claim 8, wherein the first and second type are P and N type, respectively.

10. The circuit as in claim 8, wherein the first and second voltages are Vdd and a ground voltage, respectively.

11. The circuit as in claim 8, wherein the first, fourth, fifth and sixth resistors are made of poly-silicon.

12. The circuit as in claim 8, wherein the second and third resistors are parasitic resistances of an N well.

13. A circuit for controlling a self-refresh period of a semiconductor memory device, comprising:

temperature detecting circuit outputting a temperature detection signal, comprising:

a first transistor of a first type having a source coupled to receive a first voltage;

a second transistor of the first type having a gate coupled to a gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a first bit of the temperature detection signal;

a third transistor of the first type having a gate coupled to the gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a second bit of the temperature detection signal;

a fourth transistor of a second type having a drain coupled to a drain of the first transistor;

a fifth transistor of the second type having a drain coupled to the drain of the second transistor and a source coupled to a source of the fourth transistor;

a sixth transistor of the second type having a drain coupled to the drain of the third transistor and a source coupled to the source of the fourth transistor;

a seventh transistor of the second type having a drain coupled to the drain of the fourth

transistor, a gate coupled to receive an enable signal and a source coupled to receive a second voltage; and

six resistors, with each resistor respectively coupled between the gate of the fourth transistor and the source of the first transistor, the gate of the fourth transistor and the source of the seventh transistor, the gate of the fifth transistor and the source of the first transistor, the gate of the fifth transistor and the source of the seventh transistor, the gate of the sixth transistor and the source of the first transistor, the gate of the sixth transistor and the source of the seventh transistor;

an internal period selector receiving a plurality of signals representing different periods and outputting one of the signals according to the temperature detection signal from the temperature detecting circuit;

a plurality of timers, each generating one of the signals representing the different periods; and

a self-refresh controller determining a refresh period according to the signal output from the internal period selector.

14. The circuit as in claim 13, wherein the first and second type are P and N type, respectively.

15. The circuit as in claim 13, wherein the first and second voltages are Vdd and a ground voltage, respectively.

16. The circuit as in claim 13, wherein the first, fourth, fifth and sixth resistors are made of poly-silicon.

17. The circuit as in claim 13, wherein the second and third resistors are parasitic resistances of an N well.